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(71) Applicant: 000003067

TDK Corporation

1-13-1, Nihonbashi, Chuo-ku, Tokyo

(72) Inventor: Masaaki Ikeda

c/o TDK Corporation

1-13-1, Nihonbashi, Chuo-ku, Tokyo

(72) Inventor: Nobuo Furukawa

c/o TDK Corporation

1-13-1, Nihonbashi, Chuo-ku, Tokyo

(72) Inventor: Mitsufumi Kodama

c/o TDK Corporation

1-13-1, Nihonbashi, Chuo-ku, Tokyo

(74) Agent: Attorney Kouei Yamatani, et al.

(54) [Title of the Invention]

Integrated circuit component and manufacturing method thereof

(57) [Abstract]

[Purpose]

The present invention relates to an integrated circuit component and a method for manufacturing the same. An object of the present invention is to provide an integrated circuit component in which a ceramic multilayer substrate equipped with an internal wiring or at least one kind of passive element selected from the group of L, C, and R, and a substrate equipped with an active element such as a thin film transistor are attached by a metal bump or a conductive paste to be electrically connected.

[Construction]

A metal bump or a conductive paste electrically connects between a substrate 1 where a thin film transistor is formed and a ceramic multilayer substrate 2 having an internal wiring or at least one passive element.

[Scope of Claim]

[Claim 1]

An integrated circuit component characterized by comprising:  
a glass substrate where a thin film transistor is formed; and  
a ceramic multilayer substrate equipped with an internal wiring or at least one passive element,  
wherein a metal bump or a conductive paste electrically connects between the substrates.

[Claim 2]

The integrated circuit component according to claim 1 characterized in that the electrical connection portion is filled and sealed with a non-conductive adhesive.

[Claim 3]

The integrated circuit component according to claim 2 characterized in that liquid glass is used as the non-conductive adhesive.

[Claim 4]

A method for manufacturing an integrated circuit component characterized by comprising the steps of:

adhering a non-conductive adhesive with a part left in a periphery of the electrical connection portion;

disposing it in a vacuum atmosphere; and

filling and sealing the non-conductive adhesive by gradually being replaced by an atmospheric pressure.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention]

The present invention relates to an integrated circuit component, particularly to an integrated circuit component electrically connected by adhering a ceramic multilayer substrate equipped with an internal wiring or at least one passive element and a substrate equipped with an active element such as a thin film transistor by a metal pipe or a conductive paste.

[0002]

[Prior Art]

A conventional hybrid integrated circuit is formed by, for example, mounting an active element such as a transistor manufactured in another step or an IC on a ceramic multilayer substrate having a laminated-chip shape constituting an RC network, a filter, a transformer, or the like by integrating passive elements such as a coil formed to be a thin-plate shape, a condenser, a resistor, and the like as a lamination body and providing an internal wiring.

[0003]

For example, as shown in Figure 6, there is a ceramic multilayer substrate having a laminated-chip shape where a resistor 51 having a thin-plate shape, a ceramic condenser network 52, and an internal electrode 53 are laminated on which an IC 55 provided with a Small Outline (SO) package is mounted. Note that reference numeral 54 denotes a terminal electrode; and 56, a crossover glass (for example, see *NIKKEI MICRO DEVICES*, 1990, vol. Apr., pp. 104-118).

[0004]

[Problem to be Solved by the Invention]

However, the package of the conventional SO package IC is epoxy resin or the like, and a multilayer wiring located beneath is formed from a ceramic material (including a ferrite material). Therefore, it is not rare that the linear expansion coefficient differs by about one digit. Consequently, there is a problem in reliability, in which the characteristics of the device with respect to heat shocking or a temperature cycle is likely to be deteriorated depending on the use condition.

[0005]

Further, the ceramic multilayer substrate having a laminated-chip shape, which is a complex component, and the SO package IC are manufactured under different standards. Therefore, there is a problem that the shape is bad in formability and a heteromorphic shape is formed though they are combined, and thus, the shape is difficult to be recognized by an automated packaging machine or the like such as a chip mounter.

[0006]

In addition, there is limitation on downsizing both thickness and dimension of the conventional hybrid integrated circuit in which an SO package IC is mounted on a ceramic multilayer substrate, and there is a problem in an integration degree and downsizing of the hybrid integrated circuit.

[0007]

Therefore, an object of the present invention is to provide a downsized laminated hybrid integrated circuit component having preferable formability, reliability, and an integration degree to solve the above problems.

[0008]

[Means for Solving the Problem]

In order to achieve the above object, according to the present invention, a bump made from solder metal or a conductive paste connects between a substrate such as glass over which an active element such as a thin film transistor is formed and a ceramic multilayer substrate having a laminated-chip shape over which an internal wiring or at least one passive element is formed.

[0009]

Consequently, according to the present invention, a thin film transistor is formed over a substrate such as glass. Thereafter, a connection portion is formed from a bump made from solder or gold or a conductive paste in an electrode portion over the ceramic multilayer substrate or an electrode portion of a thin film transistor which is located in the place corresponding thereto, and then, this substrate is reversed and connected to the electrode portion corresponding thereto.

[0010]

Furthermore, when the connection portion is formed from a metal bump or a conductive paste, the connection portion is gapped. Therefore, a non-conductive adhesive is attached to the connection portion to entirely depressurize to be a vacuum atmosphere with a part of this connection portion left. Then, it is gradually replaced by an atmospheric pressure and the connection portion is filled and sealed with the

non-conductive adhesive, which results in improving the reliability.

[0011]

[Effect]

Since a substrate such as glass is used as a substrate of a thin film transistor in such a manner, the linear expansion coefficient of the glass is closer to that of a ceramic multilayer substrate compared with an SO package. Therefore, a device that is resistant to heat shocking and high in reliability can be obtained.

[0012]

In addition, compared with a ceramic multilayer substrate mounting another component that is already packaged like an SO package IC, an integrated circuit component of the present invention is thin in thickness, which can realize further downsizing.

[0013]

Further, a non-conductive adhesive is penetrated and attached in a gap between the substrate and the ceramic multilayer substrate formed in a connection portion to integrate completely. Therefore, a moisture-proof effect is enhanced and the characteristics of the component are prevented from being deteriorated.

[0014]

[Embodiment]

Embodiments of the present invention are explained with reference to Figure 1 to Figure 4.

[0015]

(1) Embodiment 1

Figure 1 is a structural explanatory view of Embodiment 1 according to the present invention.

[0016]

In Figure 1, reference numeral 1 denotes a glass substrate in which a thin film transistor is formed on the surface; 2, a ceramic multilayer substrate in which a thin-film shaped internal wiring or at least one passive element is formed; 3, a bump; 4, a pad portion; and 5, a leading electrode.

[0017]

In Figure 1 (a), the glass substrate 1 in which a thin film transistor is formed and the ceramic multilayer substrate 2 in which an internal wiring or at least one passive element is formed are electrically connected to a connection portion of the internal wiring or the element in the ceramic multilayer substrate 2 and integrated by the bump 3

and the pad 4 formed on the surface of the glass substrate 1.

[0018]

Figure 1 (b) is a view in the state before connecting the glass substrate 1 and the ceramic multilayer substrate 2. A plurality of thin film transistors 7 are formed on one side and a thin film transistor IC constituting circuits such as a filter is formed over the glass substrate 1 by the combination of these thin film transistors.

[0019]

The bump 3 formed from a metal layer is formed on the glass substrate 1 over the main surface where this thin film transistor 7 is formed by transfer-screen printing or a vapor deposition method. On the other hand, when the glass substrate 1 over the ceramic multilayer substrate 2 is reversed, the pad 4 is formed in the place corresponding to the bump 3.

[0020]

During junction, pressure and heat (ultrasonic wave) are applied, if necessary.

[0021]

Next, the glass substrate 1 having the metal bump 3 is reversed over this ceramic multilayer substrate 2. Then, an integrated hybrid integrated circuit chip is formed as shown in Figure 1 (a) by overlapping the corresponding bump 3 and pad 4 and to connect the both electrically.

[0022]

Furthermore, if necessary, the leading electrode 5 is formed on the side surface of the ceramic multilayer substrate 2 and a silver-palladium terminal electrode is formed in the predetermined part over the glass substrate 1.

[0023]

However, as like in Figure 1, when the glass substrate 1 and the ceramic substrate 2 are connected by the bump, there is a gap of at least 5  $\mu\text{m}$  to 10  $\mu\text{m}$  after connecting the both. Penetrating moisture from this gap has an adverse effect, for example, aluminum or the like which is electrode metal is deteriorated.

[0024]

In order to solve these aspects, treatment as shown in Figure 2 can be carried out. In other words, liquid glass 7, for example like the commercially available OCD, is applied by an appropriate method such as blush coating to a periphery of a bump connection portion of the integrated glass substrate 1 and the ceramic multilayer substrate. At this time, a part 8 where the liquid glass is not attached to a part thereof is left (see Figure 2 (a)).

[0025]

Then, an element 10 after this integration is disposed in a bell jar 11 as shown in Figure 3, and first, it is exhausted from an exhaust port 12 to be a vacuum.

[0026]

After exhausting into a vacuum, gas is gradually flown from an air-intake 13 to be replaced by an atmospheric pressure.

[0027]

In this process, the bump connection portion between the glass substrate 1 and the ceramic multilayer substrate 2 is filled with the liquid glass 7 in airtight, and there is no gap therebetween.

[0028]

Next, surplus liquid glass, especially liquid glass covering a surface electrode over the thin film transistor or the leading electrode 5 of the ceramic multilayer substrate 2 is removed. Thereafter, baking is carried at temperatures from 450°C to 800°C, a glass layer 7' is formed, and then, the glass substrate and the ceramic multilayer substrate 2 are integrated by completing filling and sealing (see Figure 2 (b)).

[0029]

After the integration, the leading electrode 5 of the ceramic multilayer substrate 2 and, if necessary, a pad electrode of the thin film transistor 7 are exposed by etching, a silver-palladium electrode material is applied, and baking is carried out at temperatures 500°C or less to form a terminal electrode.

[0030]

## (2) Embodiment 2

In another embodiment of the present invention, a substrate 1 where a thin film transistor is formed and a ceramic multilayer substrate 21 are integrated not by a bump but by an extraction terminal 23 made from a conductive paste.

[0031]

Figures 4 (a) and (b) show the examples thereof. In the ceramic multilayer substrate 21 in Figure 4, an internal wiring or at least one passive element selected from the group of L, C, and R is formed as is shown in the cross-sectional views in Figures 4 (a) and (b).

[0032]

In Figure 4 (a), a condenser portion 24 and a wiring portion 25 are formed in the ceramic multilayer substrate 21 made from glass ceramic or the like by an internal wiring layer 22 made from silver-palladium, and the extraction terminal 23 is formed on

the surface. Reference numeral 1 denotes a glass substrate where a thin film transistor is formed; and 7', a glass layer.

[0033]

Figure 4 (b) is the case using a ceramic multilayer substrate 21 internally equipped with an internal wiring layer 22, and in the same manner, the extraction terminal 23 of silver-palladium is formed on the surface and is connected to a TFT of the glass substrate 1 with a conductive paste 24.

[0034]

Note that Figures 5 (a), (b), and (c) show an example of a laminated LC chip constituting a filter as an example of such a ceramic multilayer substrate.

[0035]

Figure 5 (a) is a perspective view of the laminated LC chip, Figure 4 (b) is an example of the internal intersected circuit, and Figure 4 (c) is an internal structural explanatory view of an inductor (L) used for the transformer portion.

[0036]

In Figure 5, reference numeral 41 denotes a condenser network portion; 42, a transformer portion; 43, an internal conductor; 44, an external electrode; 45, a leading electrode; and 46, a terminal electrode.

[0037]

Note that, in these embodiments, an example using a glass substrate as a substrate where a thin film transistor is formed is explained; however, the present invention is not limited thereto as long as a substrate which has a linear expansion coefficient close to a ceramic material and a thin film transistor can be formed, is employed.

[0038]

In addition, an example using liquid glass as a non-conductive adhesive that seals a connection portion such as a bump is explained; however, the present invention is not limited thereto, and epoxy resin, silicon resin, and contractile resin can be also used as long as they are non-conductive adhesives.

[0039]

Furthermore, in the above embodiment, a manufacturing process of a chip, which is a component, is shown with reference to the figures, and mass production is possible according to the present invention.

[0040]

In this case, by using a large ceramic substrate, which is easily treated, a glass



substrate where a thin film transistor is formed is disposed and connected thereto. Thereafter, a plurality of elements can be obtained at once by cutting the substrate vertically and horizontally with the use of a dicing saw.

[0041]

[Effect of the Invention]

A thin film transistor of the present invention is formed over a substrate, such as a glass substrate, of which linear expansion coefficient is closer to that of a ceramic multilayer substrate, compared with an SO package. Therefore, it is resistant to heat shocking or a temperature cycle, and thus, the high reliability can be obtained.

[0042]

In addition, since a thin film transistor before being provided with an SO package is integrated with a passive element or the like, it largely contributes to downsizing.

[0043]

According to the present invention, in an integrated circuit component in which a thin film IC portion and a laminated chip are connected by a metal bump, a bump connection portion can be filled and sealed with a non-conductive adhesive and a moisture-proof effect is enhanced further, and thus, deterioration in characteristics can be prevented.

[0044]

A downsized, lightweight, high-reliable, multifunctional, and low-cost integrated circuit component thus manufactured can be obtained and automated packaging is easily carried out. Therefore, the integrated circuit component can be employed for various electronic components such as a filter computer delay line, a general-purpose logic circuit, a DC-DC converter, an electronic switch, or an audio filter.

[Brief Description of Drawings]

Figure 1 is a structural explanatory view and a manufacturing process explanatory view of an embodiment according to the present invention.

Figure 2 is a manufacturing process explanatory view of an embodiment according to the present invention.

Figure 3 is a schematic view of a manufacturing device of an embodiment according to the present invention.

Figure 4 is a structural explanatory view of another embodiment according to the present invention.

Figure 5 is an example of a structural explanatory view of a ceramic multilayer

substrate.

Figure 6 is a perspective view of a conventional example.

[Description of the References Symbols]

1 glass substrate

2 ceramic multilayer substrate

3 bump

4 pad

5 leading electrode